

**FIG. 1**

FIG. 2 is a block diagram of a bus control logic circuit. The circuit includes a data input 205, a strobe input 210, and a bus control logic 125. The bus control logic 125 includes a state machine 220, a glitch detector 230-1, a glitch indicator 230-2M, a reset logic 244, and a data latch 250. The data input 205 is connected to the data latch 250 via a bus 207. The strobe input 210 is connected to the state machine 220 via a bus 210. The state machine 220 is connected to the glitch detector 230-1 and the reset logic 244. The glitch detector 230-1 is connected to the glitch indicator 230-2M. The glitch indicator 230-2M is connected to the reset logic 244. The reset logic 244 is connected to the data latch 250. The data latch 250 is connected to the bus 207. The bus control logic 125 also includes a set of data latches 215-1 to 215-N, each with its own clock input (CLK1 to CLKN) and a common data input (DATA). The data latches 215-1 to 215-N are connected to the bus 207 via a multiplexer 240. The multiplexer 240 is connected to the data latch 250. The bus control logic 125 also includes a set of internal non-overlapping clocks 232, which are connected to the data latches 215-1 to 215-N. The bus control logic 125 also includes a set of TO/FROM BUS CONTROL LOGIC 245, which is connected to the data latch 250.

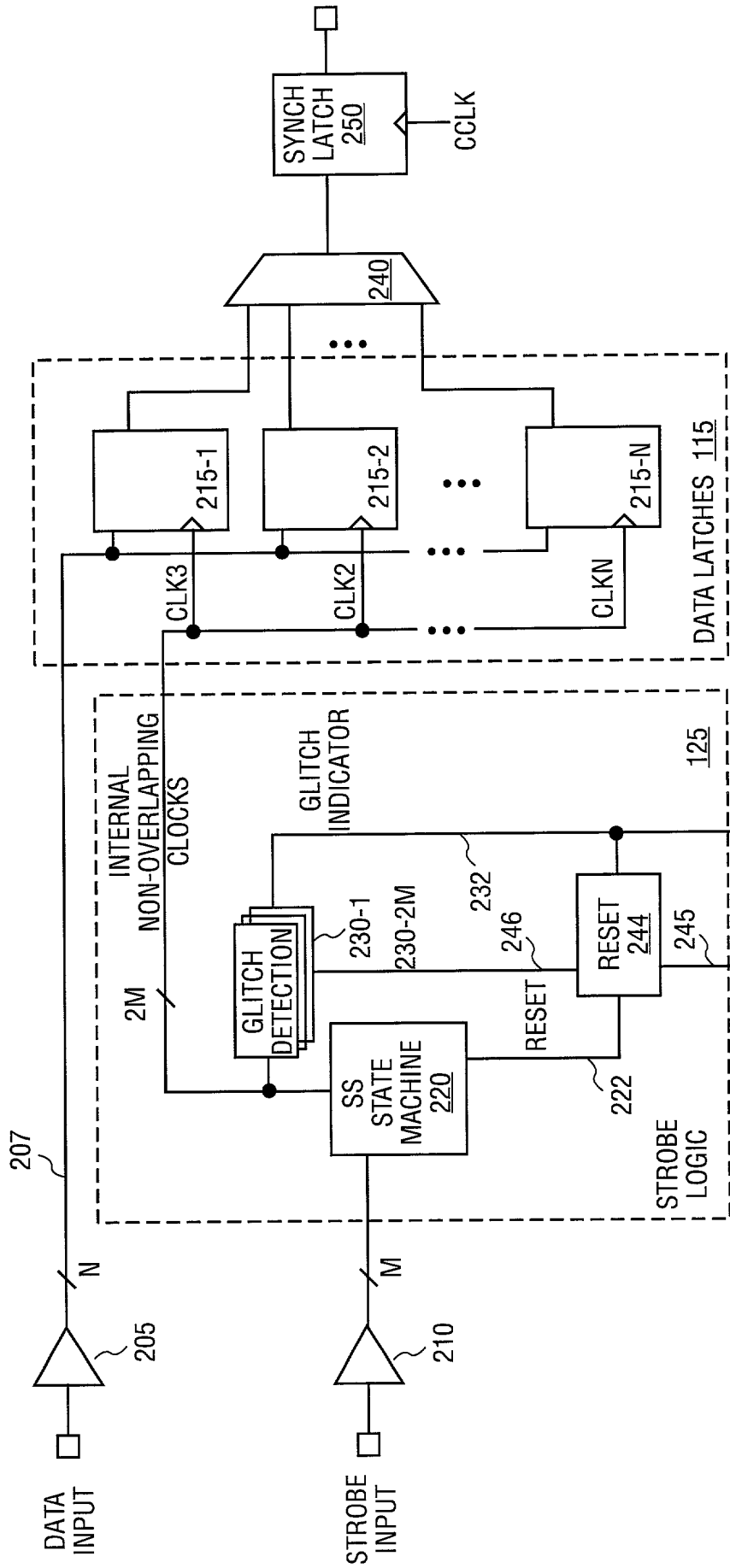


FIG. 2

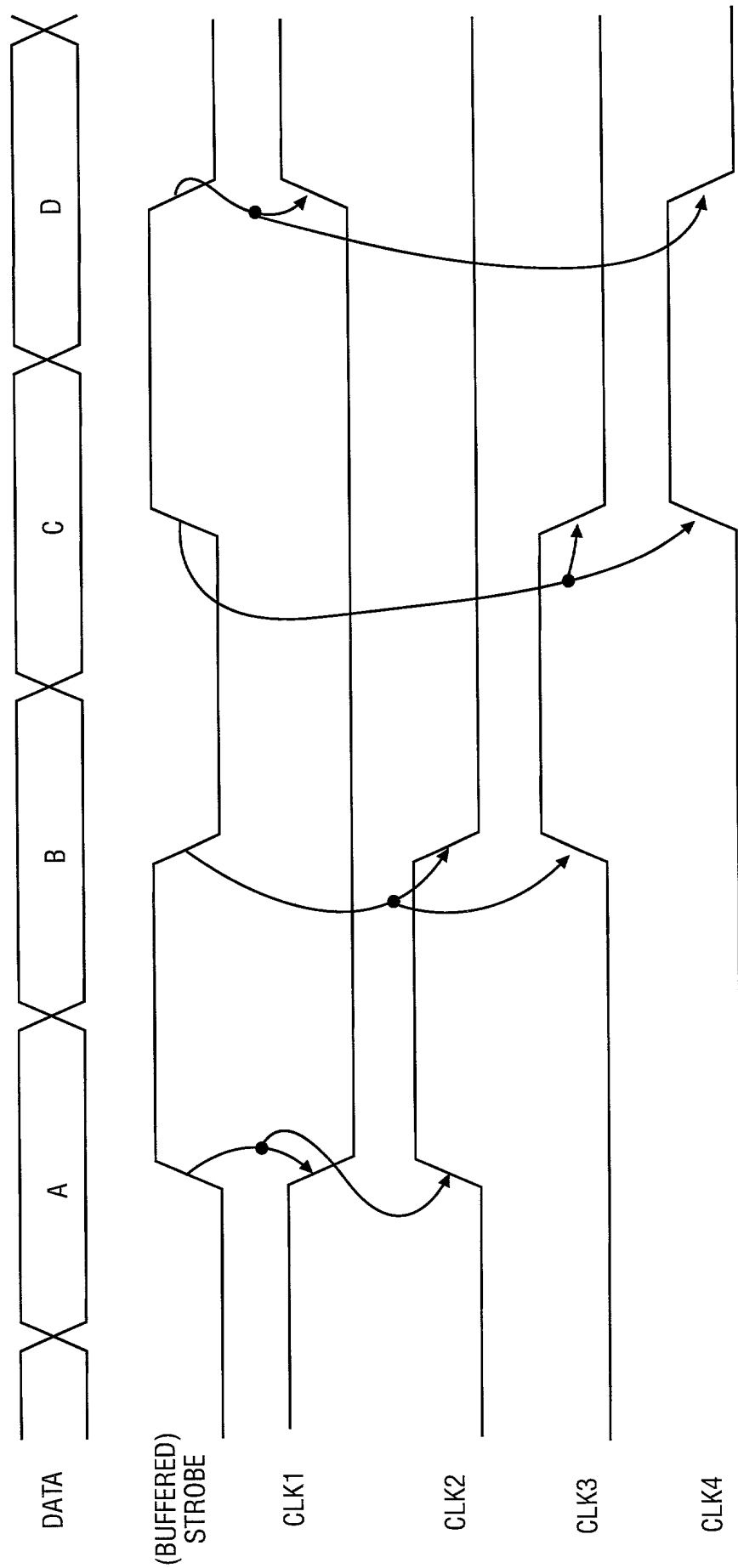


FIG. 3

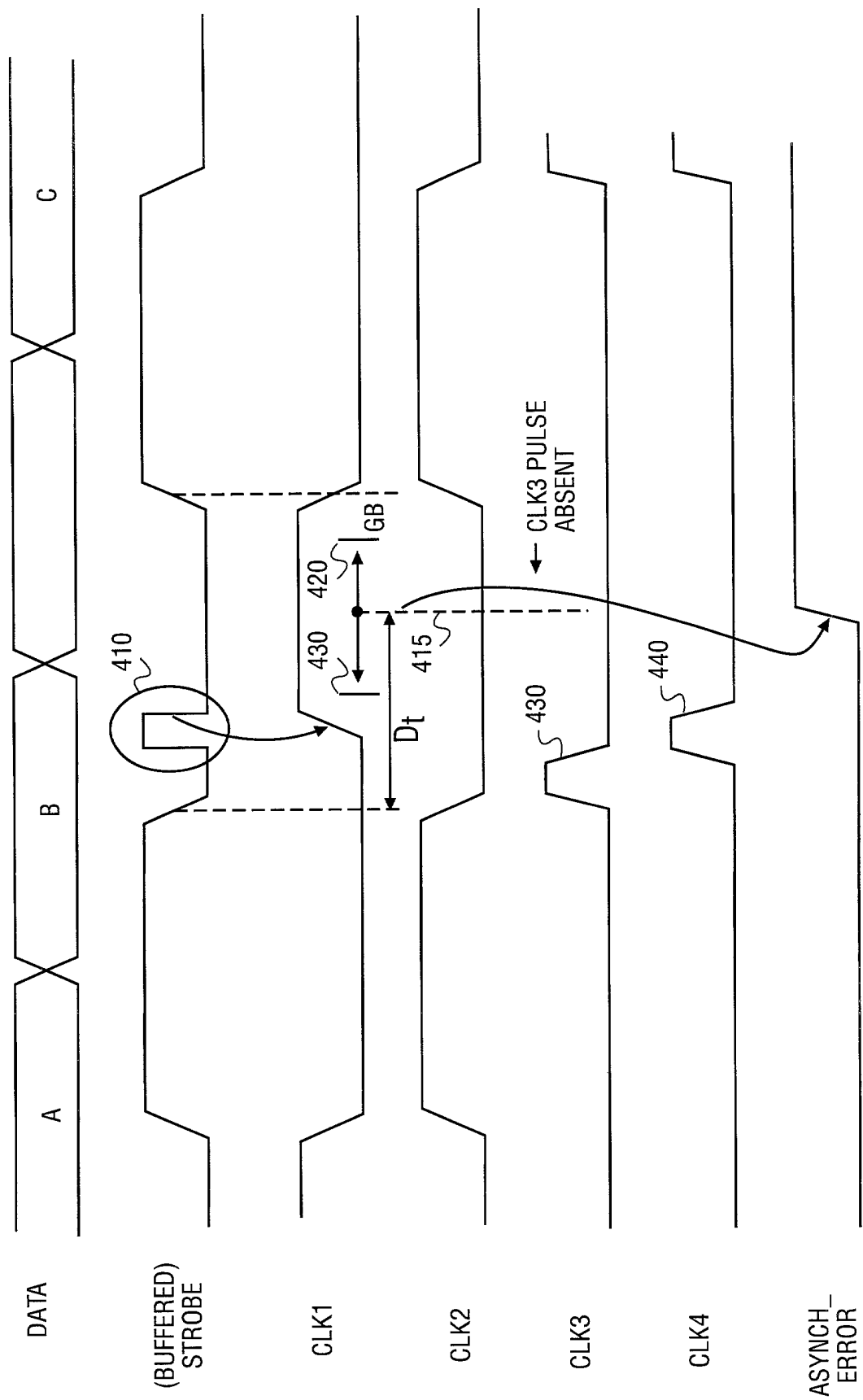


FIG. 4

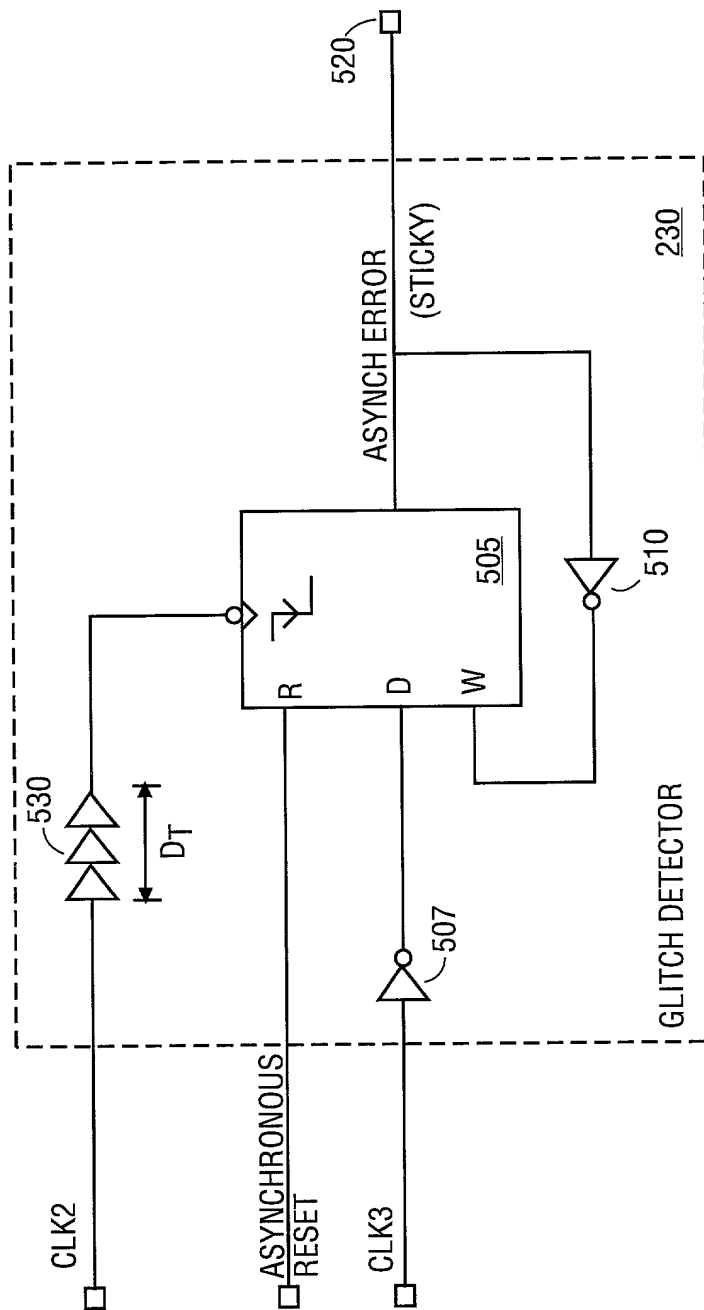


FIG. 5

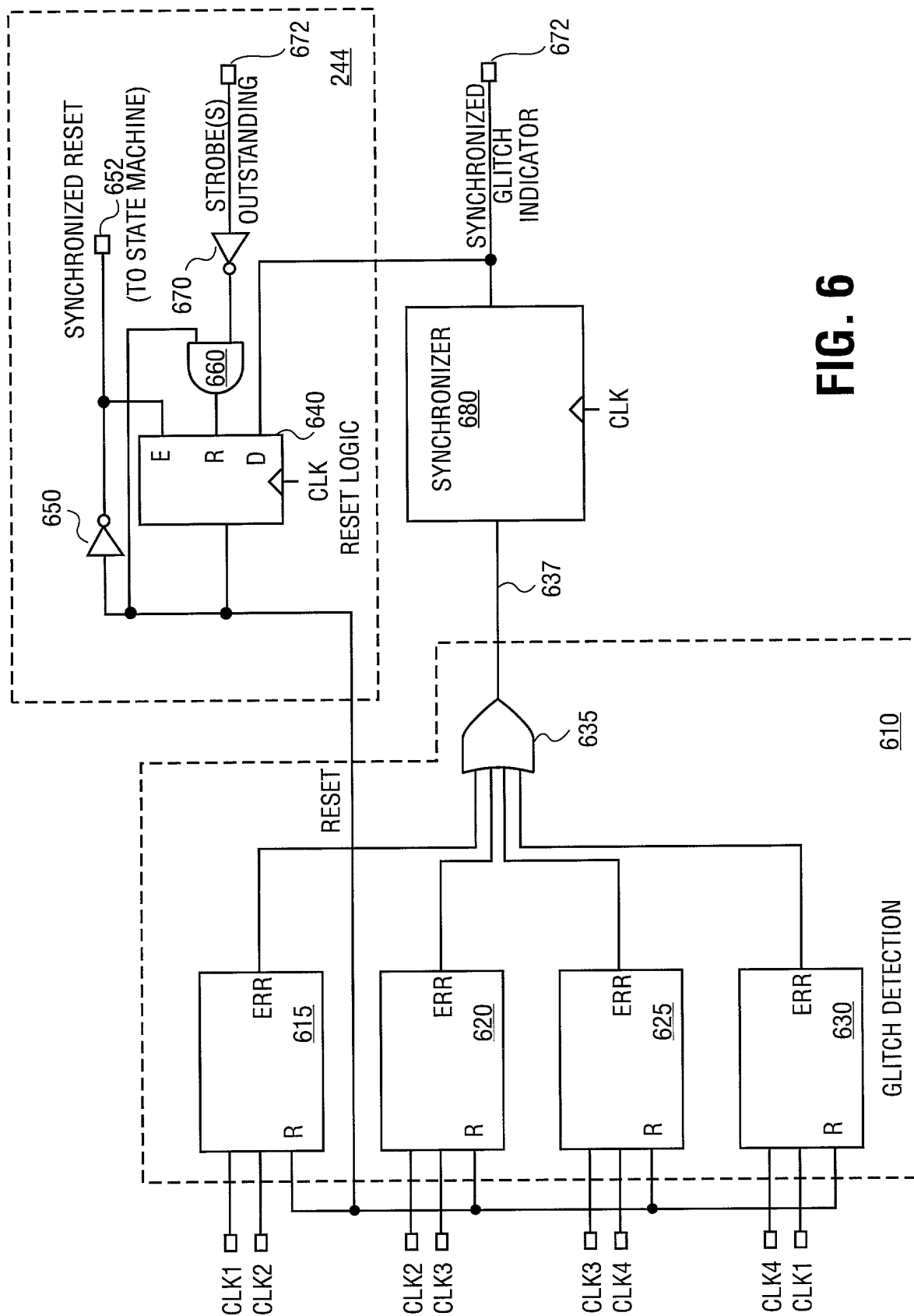


FIG. 6